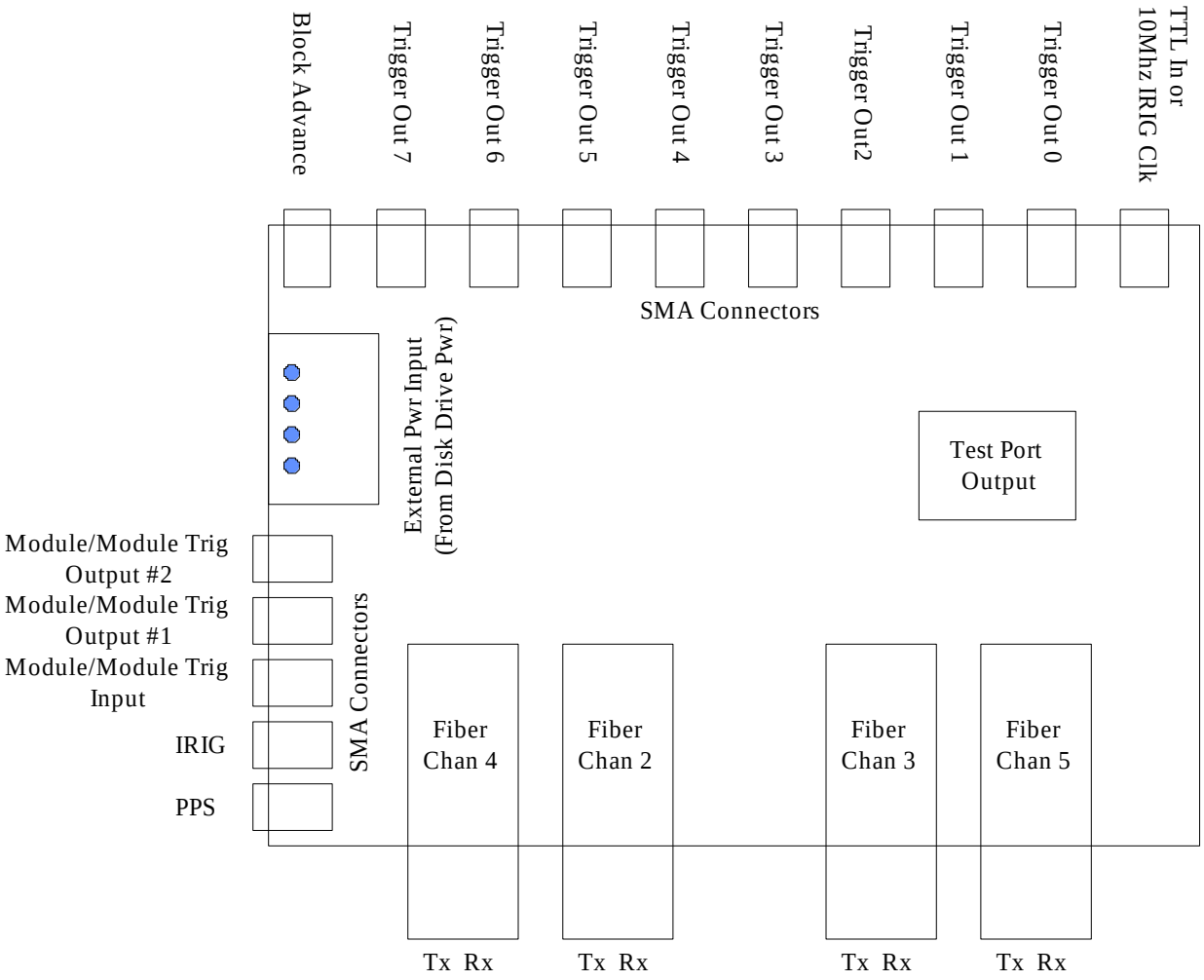
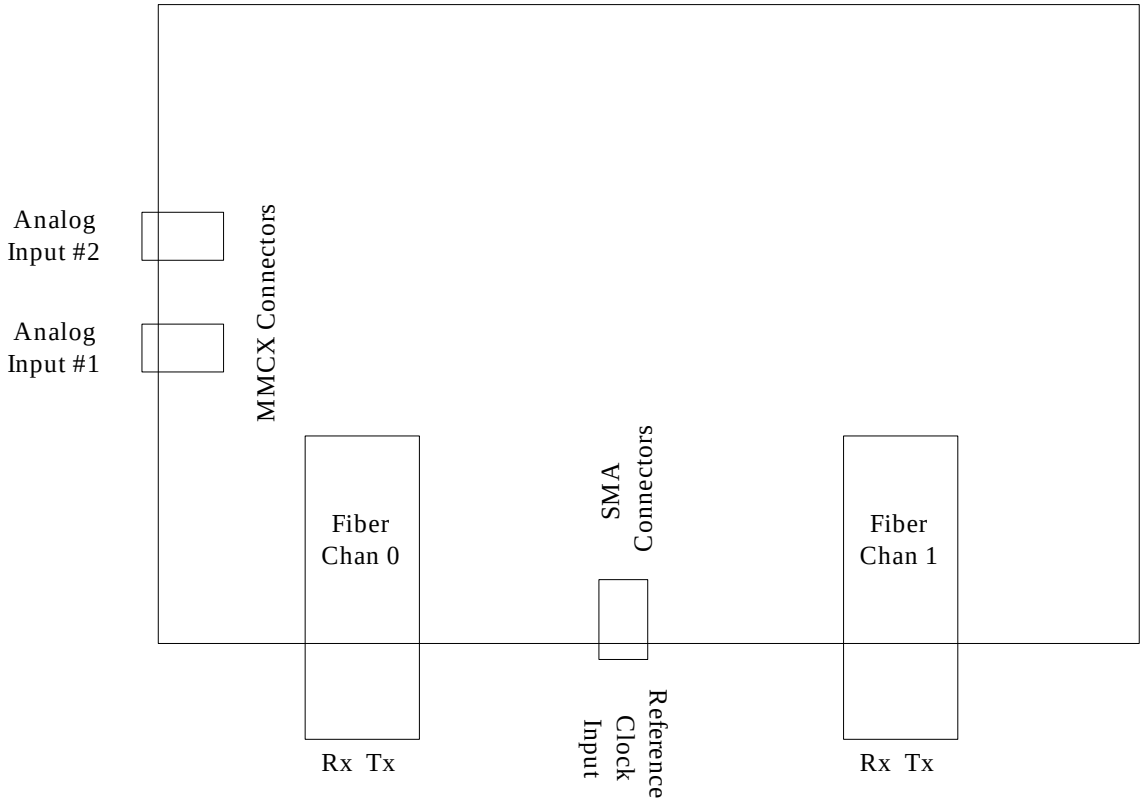
Fiberlizer
Receive (Rx) Operation User's Guide

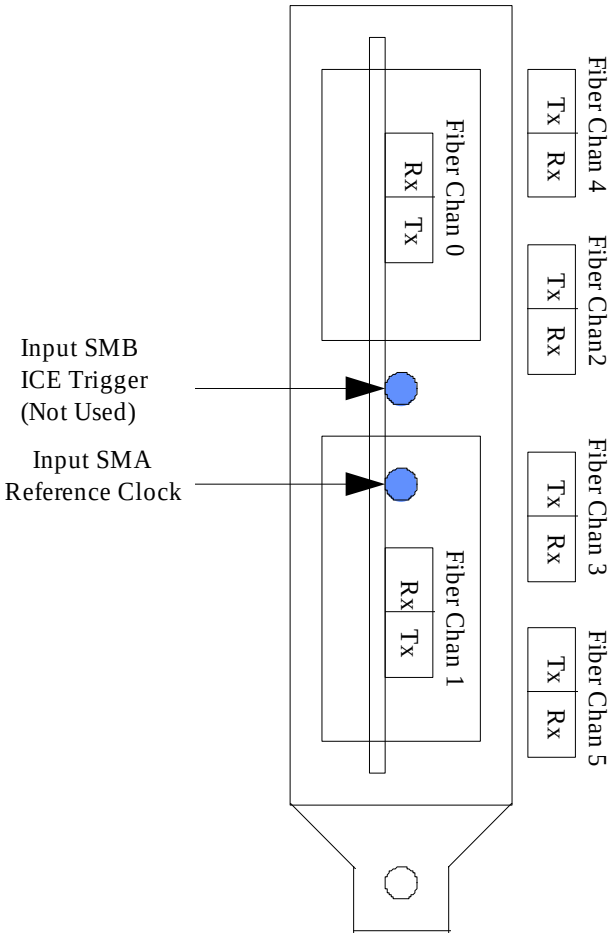
Ports:



Fiberlizer-Sub Module
Top View
(As Assembled On Card)



Fiberlizer-Module
Top View
(As Assembled On Card)



PCI Bracket/Fiber
Edge View

Hardware Ports for Module Rx Mode:

Signals	Direction	In Use
TRG7-TRG0	Trigger Outputs	No **
BLKA	Trigger Output	No
TestPt7-TestPt0	Test Point Outputs	No **
ModTrigOut2-ModTrigOut1	Trigger Outputs	No
ModTrigIn	Trigger Input	No
10MHz Clock	IRIG Clock Input	No
IRIG	IRIG Data Input	No
PPS	IRIG PPS Input	No
Disk Power Connector	Power Input	Yes
Fiber Receivers5-0	Fiber Input	Yes
Fiber Transmitters	Fiber Output	No **
Reference Clock	Clock Input	Yes *

*In Use Depending On Module Firmware Download
** In Use When Module Configured In Output Mode
Note-Signals note used when the module is configured for input and output are available and reserved for use with future Fiberlizer FPGA firmware downloads

For use of all 6 fiber channels external power must be applied to sub-module. This power connection is a standard Molex hard drive power power connection that can be found inside computers. Simply attached the power connection prior to powering up the system.

Software Module Designation:

Input: FLZRXDR1
Output: DXFLZRR1

Fiberlizer Downloads:
iceflzrxdr1_ext.prm
iceflzrxdr1_osc1600.prm
iceflzrxdr1_osc800.prm
iceflzrxdr1.prm

Currently the Fiberlizer comes with 3 downloads. All downloads have the prefix “iceflzrxdr1” the remaining characters of the file name describe the downloads use of a clock source for clock and data recovery. _osc1600 means that the Fiberlizer will use its on-board reference to lock to a 1600Mhz input fiber signal. _osc800 means that the Fiberlizer will use its on-board reference to lock to a 800Mhz input fiber signal. _ext means that the Fiberlizer will use an external reference in the range of 400MHz to 1600Mhz to lock to an incoming fiber signal of the same rate as the input reference.

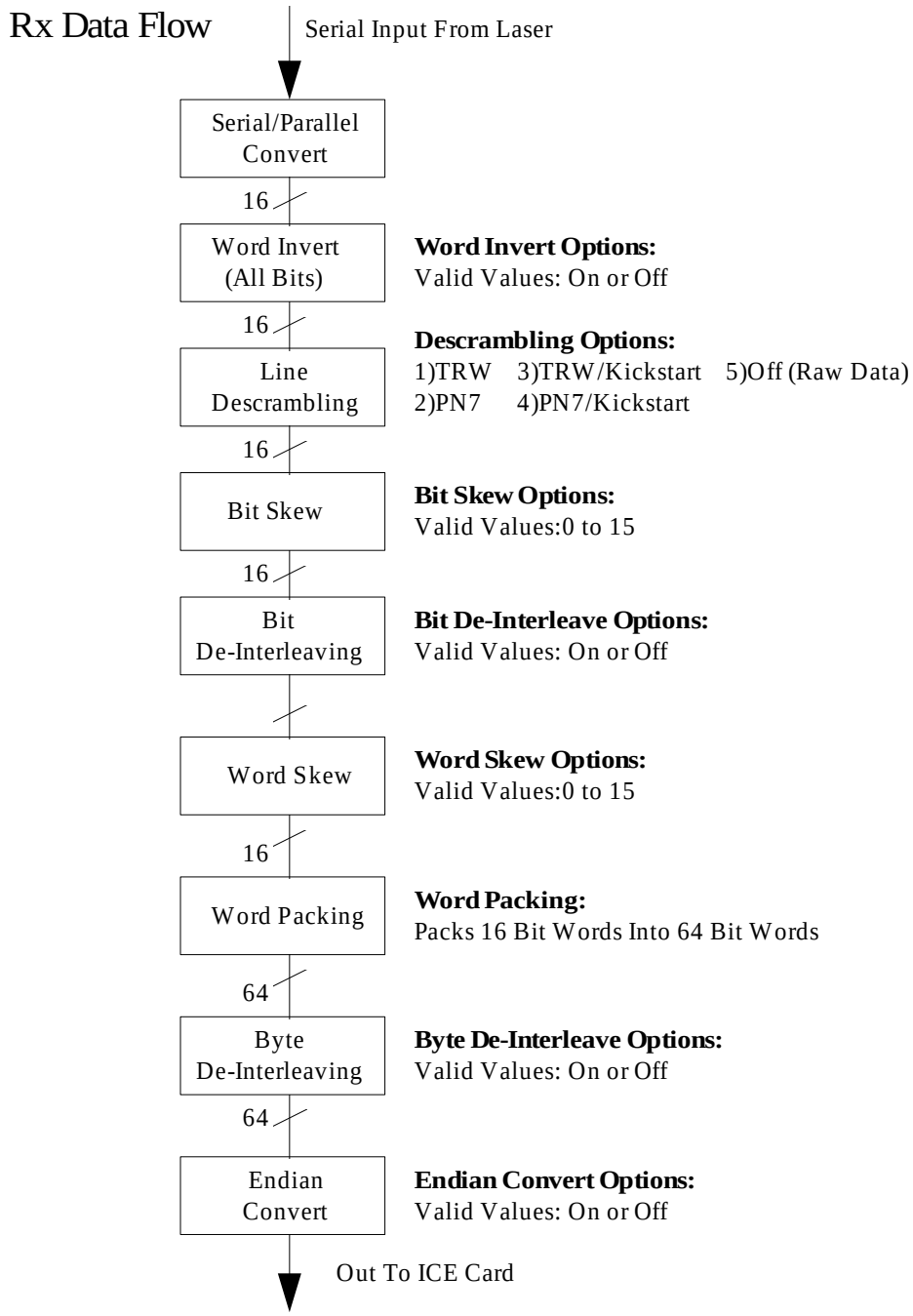
Use of the flag IOMFPGA=<string> will allow the user to download the needed FPGA firmware to the module. Where string is “_osc1600”, “_osc800”, or “_ext” Note that upon power up the FPGA of the Fiberlizer does not contain a download. Upon the first reset of the ICE PCI card, the absence of a download in the Fiberlizer is detected and the download iceflzrxdr1.prm is sent to the module. This download is a duplicate of the download file iceflzrxdr1_ext.prm Therefore, without specifying the flag IOMFPGA=<string> the default download of the module will be to use and external clock as its fiber line rate reference. Using the flag IOMFPGA=<string> will allow you to choose the download for the first reset of the ICE PCI card and Fiberlizer module.

Finally, if the Fiberlizer module has previously been downloaded with firmware, new firmware will NOT be downloaded automatically by specifying the flag IOMFPGA=<string>. The ICE PCI card detects the presence of a previous download and ignores the flag IOMFPGA=<string>. To override this feature use the FORCE flag in conjunction with the flag IOMFPGA=<string> flag. This will force the new firmware to be downloaded into the module.

Examples For C:
#define ICEDEV1 "ICEPIC,DEVNO=0,IOM=FLZRXDR1,IOMFPGA=_osc1600,FORCE,,"

Examples For Nextmidas/Xmidas
picd/flags=iom=flzrxdr1|force| iomfpga=osc1600 reset pic1

Rx Logic Block:



Some of the above options are available on a per fiber basis. Other options apply to all the data from the module.

Options available per fiber: Word Invert, Bit Skew, Word Skew

Options on all data: Descrambling, Bit De-Interleave, Byte De-Interleave, Endian Conversion

Options available per fiber

Options available on a per fiber basis are configured by writing to transceiver configuration registers that are assigned to each fiber transceiver block. This is accomplished via software "setkey" calls from either a C program or Xmidas/Nextmidas applications. Note that these configuration register writes are never cleared from acquisition to acquisition unless overwritten by the user or the module is re-loaded with its firmware.

32 Bit Configuration Register:

Bit 0 is the LSBit and bit 31 is the MSBit.

Most Significant Bits:

Bits 31 and 30 must be set to 1.

Channel Number:

Bits 29 to 27 hold a value of 0 (000b) to 5 (101b) representing which channel is to be configured.

Register ID:

Bits 26 to 16 are the register ID. These are binary encoded. In other words, there should never be more than 1 bit set among these 10 bits.

Bits 26 to 16
0000000001b – Write to Bit Shift Register
0000000010b - Unused for Rx Operations
0000000100b - Write to Word Invert Register
0000001000b – Write to Word Shift Register
All other values unused.

Register Values:

Bit Shift Register-4 bit register. Valid values are 0000h to 000Fh and represent the number of bits to shift the data. Value at the time of the FPGA firmware download is 0000h

Word Invert Register-1 bit register. Valid values are 0000h or 0001h. A value of 0001h will invert all data. A value of 0000h will disable inverting the data. Value at the time of the FPGA firmware download is 0000h

Word Shift Register-4 bit register.Valid values are 0000h to 000Fh and represent the number of 16 bit words to shift the data. Value at the time of the FPGA firmware download is 0000h

Per Fiber Register Access:

From a C application, access to the fiber registers is accomplished using a call to the setkey() function with the flags KEY_MOD.

dmac is the DMA channel that is returned from a call to pic_ioport()
p1 is a pointer to the pic card structure.
reg_bits is the 32 bit value as described above for a configuration register.
pic_setkeyl(p1, dmac, KEY_MOD, reg_bits);

From an Xmidas/Nextmidas application, access to the fiber registers is accomplished using a call to the setkey() using the pic driver interface.

picd/port=module2/flags=iom=flzrxdr1/hex set pic1 mod <value>

Note that the setkey operation must always be performed on module 2. The key of "mod" will instruct the ICE PCI card to send <value> to the Fiberlizer module. <value> is listed as a 32 bit hex number. An example is 0xC0010001. This value will configure the Bit Shift register of fiber 0 to shift the data by 1 bit.

Options on all data

Options available on all fiber channels will global change data for all 6 fiber inputs. The options available are Descrambling, Bit De-Interleave, Byte De-Interleave, and Endian Conversion. These option apply to all 6 fiber inputs. The use of each if controlled through the use of "flags" that are passed in via the PIC open string in a C application or via the flags that are passed into a call to source_pic or pic_driver when using an Xmidas/Nextmidas application.

Flags:

ENDCNV	Endian Convert 32 Bit Data
DISINTLV	Disable Bit De-Interleaving
DISSTRMINTLV	Disable Stream/Byte De-Interleaving
SCRAMOFF	Turn Off Descrambling of Fiber Data
PN7SCRAM	Enable PN7 Descrambling
KICKEN	Turn On Kickstart Circuit For PN7 or TRW De-Scrambling
CHANCFGVAL = <value>	Bit Encoded Channels To Acquire

The flag CHANCFGVAL=<value> sets the number of channels to acquire. The <value> parameter represents the bit encoded channels to be acquired. For example, if only channel 0 is to be acquired the <value> is 1. If channel 5 is to be acquired then <value> is 32. If channels 2 and 3 are to be acquired then <value> is 12. If all channels are to be acquired then <value> is 63.

By default the Fiberlizer assumes that the fiber data is 2 streams of data running at half the line rate that is interleaved at the source to produce the full line rate that is then output on the fiber. With this default acquisition data is de-interleaved and each of the 2 streams is placed into 32 bits of data to form a 64 bit value. The most significant 32 bits is from one stream and the least significant 32 bits is from the 2nd stream. Below is an example of fiber data that consists of alternating 1's and 0's.

10101010101010101010101010101010
First Arrival Line Data Last Arrival

The output data would then appear as:

1 Channel Acquisition
with Bit Shift = 0

Addr 0	0xFF
Addr 1	0xFF
	0xFF
	0xFF
	0x00
	0x00
	0x00
	0x00
	0xFF
	0xFF
	0xFF
	0xFF
	0x00
	0x00
Addr 14	0x00
Addr 15	0x00

By using the Bit shift register a user could change the stream alignments.

1 Channel Acquisition
with Bit Shift = 1

Addr 0	0x00
Addr 1	0x00
	0x00
	0x00
	0xFF
	0xFF
	0xFF
	0xFF
	0x00
	0x00
	0x00
	0x00
	0xFF
	0xFF
Addr 14	0xFF
Addr 15	0xFF

The above depictions show how data will be stored in ICE PCI card DMA memory on the host computer. Note that each 32 bits represents a stream of data that is ½ the line rate. By using the flags DISINTLV and DISSTRMINTLV together a user can get “raw” line data. By default the Fiberlizer assumes that the line data is interleaved and needs to be de-interleaved and placed in 32 bit samples.

Below are diagrams showing how multiple channels would appear in ICE DMA memory. Note for multiple channels acquisitions using the flags DISINTLV and DISSTRMINTLV data would appear as 64 bits from the 1st channel, 64 bits from the 2nd channel, and so on. It would then be up to the user to pull out 64 bits of data at a time for each channel that is acquired.

1 Channel Acquisition
1st CH Stream A Byte 0
1st CH Stream A Byte 1
1st CH Stream A Byte 2
1st CH Stream A Byte 3
1st CH Stream B Byte 0
1st CH Stream B Byte 1
1st CH Stream B Byte 2
1st CH Stream B Byte 3
1st CH Stream A Byte 0
1st CH Stream A Byte 1
1st CH Stream A Byte 2
1st CH Stream A Byte 3
1st CH Stream B Byte 0
1st CH Stream B Byte 1
1st CH Stream B Byte 2
1st CH Stream B Byte 3

1 Channel Acquisition Endian Converted
1st CH Stream A Byte 3
1st CH Stream A Byte 2
1st CH Stream A Byte 1
1st CH Stream A Byte 0
1st CH Stream B Byte 3
1st CH Stream B Byte 2
1st CH Stream B Byte 1
1st CH Stream B Byte 0
1st CH Stream A Byte 3
1st CH Stream A Byte 2
1st CH Stream A Byte 1
1st CH Stream A Byte 0
1st CH Stream B Byte 3
1st CH Stream B Byte 2
1st CH Stream B Byte 1
1st CH Stream B Byte 0

2 Channel Acquisition
1st CH Stream A Byte 0
1st CH Stream A Byte 1
1st CH Stream A Byte 2
1st CH Stream A Byte 3
1st CH Stream B Byte 0
1st CH Stream B Byte 1
1st CH Stream B Byte 2
1st CH Stream B Byte 3
2nd CH Stream A Byte 0
2nd CH Stream A Byte 1
2nd CH Stream A Byte 2
2nd CH Stream A Byte 3
2nd CH Stream B Byte 0
2nd CH Stream B Byte 1
2nd CH Stream B Byte 2
2nd CH Stream B Byte 3

3 Channel Acquisition
1st CH Stream A Byte 0
1st CH Stream A Byte 1
1st CH Stream A Byte 2
1st CH Stream A Byte 3
1st CH Stream B Byte 0
1st CH Stream B Byte 1
1st CH Stream B Byte 2
1st CH Stream B Byte 3
2nd CH Stream A Byte 0
2nd CH Stream A Byte 1
2nd CH Stream A Byte 2
2nd CH Stream A Byte 3
2nd CH Stream B Byte 0
2nd CH Stream B Byte 1
2nd CH Stream B Byte 2
2nd CH Stream B Byte 3
3rd CH Stream A Byte 0
3rd CH Stream A Byte 1
3rd CH Stream A Byte 2
3rd CH Stream A Byte 3
3rd CH Stream B Byte 0
3rd CH Stream B Byte 1
3rd CH Stream B Byte 2
3rd CH Stream B Byte 3

The 2nd diagram shows a representation of the data when the flag ENDCNV is used to change the data representation from “little endian” format to “big endian” format.

Line Descrambling:

By default the Fiberlizer expects the fiber line data to be scrambled using the TRW scrambling method. By adding the flag KICKEN the user can then specify that the line data is TRW with Kickstart scrambled and should be descrambled accordingly. Use of the flag PN7SCRAM turns off the TRW descrambler and enables the PN7 descrambler. Using both the PN7SCRAM and KICKEN flags turns on the PN7 descrambler with Kickstart enabled. Finally, using the flag SCRAMOFF turns off all line descrambling and brings in raw scrambled line data.

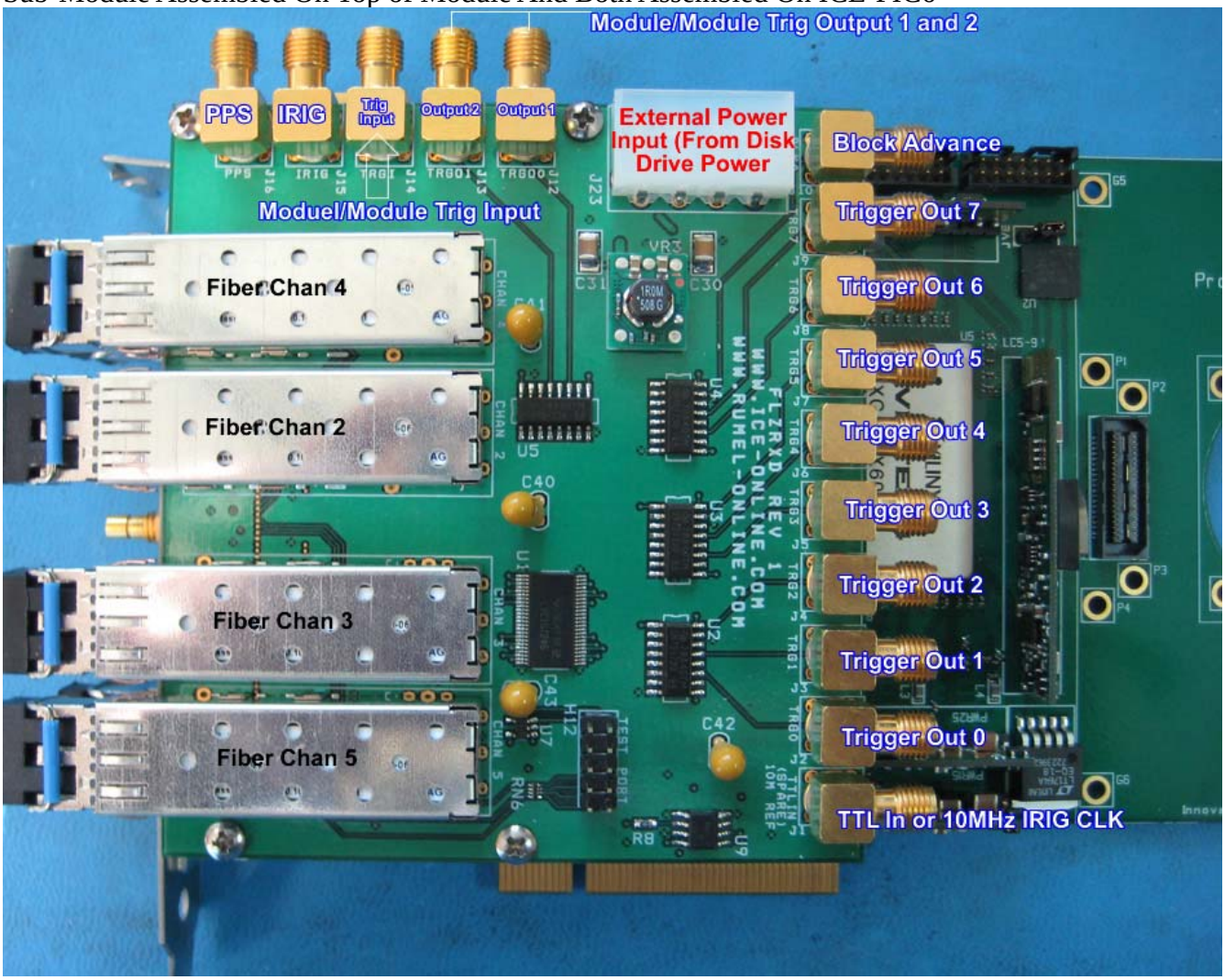
ICE Software Interface:

When acquiring data from either a C application the parameters for port number and data size should be set to module 3 and data size = -8. This represents acquiring data from both module ports with a data size of complex byte. The data rate should be set to a value that is equal to the total number of channels times the line rate divided by 16. For instance, 6 channels of fiber data running at 1600Mhz would be a data rate of 6 * 1600M/16 = 600,000,000. This is the value that should be passed in as the data rate.

When using Xmidas/Nextmidas application the same parameters apply. Port number should always be 3 and the data size should be complex byte. Data rate calculations should be calculated as directed above.

Sub-Module (Detached)

Sub-Module Assembled On Top of Module And Both Assembled On ICE-PIC6



External View Outside Chassis (Note Channel Numbers, Rx & Tx Connections On Transceivers)